ABSTRACT OF THE DISCLOSURE

An embodiment of the invention is a floating point flag combining or accumulating circuit comprising an analysis circuit that receives a plurality of floating point operands, each having encoded status flag information, and a result assembler. The analysis circuit analyzes the plurality of floating point operands and provides an indication of one or more predetermined formats in which the plurality of floating point operands are represented. The result assembler receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from at least two of the plurality of floating point operands.